MEMORY CIRCUITS AND METHODS OF MAKING AND DESIGNING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims the benefit of U.S. Provisional Application Ser. No. 61/576,254, filed on Dec. 15, 2011, the contents of which are incorporated by reference herein, in their entirety.

TECHNICAL FIELD

The present invention relates generally to memory circuits and methods, and more particularly to latch based memory circuits with high body effect transistors, and methods of designing memory cells.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1**A is a side cross sectional view showing a deeply depleted channel (DDC) transistor that can be included in embodiments.

FIG. **1**B is a side cross sectional view showing various transistor types that can be included in embodiments.

FIG. **1**C is a flow diagram showing methods of fabricating DDC transistors according to embodiments.

FIGS. **2**A-**0** and **2**A-**1** are diagrams of a storage circuit and transistors therefor, according to embodiments.

FIG. **2**B is a block schematic diagram of a static random access memory (SRAM) device according to an embodiment.

FIG. **3**A is a block schematic diagram of a SRAM device according to another embodiment.

FIG. **3**B is a block schematic diagram of a SRAM device according to a further embodiment.

FIG. **3**C shows read and write failure rates for an SRAM cell at different stages of a design process to reduce VDDmin.

FIG. **4**A is a flow diagram of a method according an embodiment.

FIG. **4**B is a diagram showing threshold variations candidates that can be evaluated in a method like that of FIG. **4**A.

FIG. **5**A is an isoplot of bit failure rates for an SRAM device according to one embodiment.

FIG. **5**B is an isoplot of bit failure rates for the SRAM device of FIG. **5**A at a lower power supply voltage, according to one embodiment.

DETAILED DESCRIPTION

Various embodiments of the present invention will now be described in detail with reference to a number of drawings. The embodiments show circuits and methods related to an integrated circuit device having transistors that have an enhanced body coefficient. The embodiments described herein also show circuits and methods related to an integrated circuit having improved transistor matching, such that the transistors have reduced variability of threshold voltage and body coefficient. Particular embodiments may include latch type memory elements, such as static random access memories (SRAMs) having enhanced cell stability and capable of operation at reduced power supply voltages, as compared to SRAMs employing conventional transistors.

FIG. **1**A shows an embodiment of a deeply depleted channel (DDC) transistor **100** that is configured to have an enhanced body coefficient, along with the ability to set a threshold voltage (Vt) with enhanced precision, according to certain described embodiments. The DDC transistor **100** includes a gate electrode **102**, source **104**, drain **106**, and a gate dielectric **128** positioned over a substantially undoped channel **110**. In the embodiment shown, lightly doped source and drain extensions (SDE) **132**, positioned respectively adjacent to source **104** and drain **106**, extend toward each other, reducing effective length of the substantially undoped channel **110**. In alternate embodiments, a DDC transistor may not include SDEs **132**.

In FIG. **1**A, the DDC transistor **100** is shown as an N-channel transistor having a source **104** and drain **106** made of N-type dopant material, formed upon a substrate such as a P-type doped silicon substrate providing a P-well **114** formed on a substrate **116**. In addition, the N-channel DDC transistor in FIG. **1**A includes a highly doped screening region **112** made of P-type dopant material, and a threshold voltage set region **111** made of P-type dopant material. However, it will be understood that, with appropriate change to substrate or dopant material, a p-channel DDC transistor can be formed from suitable substrates.

In one embodiment, a process for forming the DDC transistor begins with forming the screening region **112**. In certain embodiments, the screening region **112** is formed by implanting dopants into the P-well **114**. In alternative embodiments the screening region is formed on the P-well using methods such as in-situ doped epitaxial silicon deposition, or epitaxial silicon deposition followed by dopant implantation. The screening region formation step can be before or after the formation of isolation structures, such as STI (shallow trench isolation) formation, depending on the application and results desired. Boron (B), Indium (I), or other P-type materials may be used for P-type implants, and arsenic (As), antimony (Sb) or phosphorous (P) and other N-type materials can be used for N-type implants. In certain embodiments, the screening region **112** can have a dopant concentration between about 1×10^{19} to 5×10^{20} dopant atoms/cm^3, with 5×10^{19} being typical, the dopant concentration being selected to achieve the desired characteristics of the transistor such as reductions in drain induced barrier lowering (DIBL), on and off current (Ion vs. Ioff) and so on, with the concentration sufficiently high to effectively pin the depletion width of the channel for a given gate voltage. A carbon (C), or other dopant migration resistant layer can be applied above the screening region to reduce upward migration of dopants, particularly to inhibit the migration of boron dopants. Preferably, the carbon is preceded by a germanium implant to facilitate the traveling of the carbon atoms into lattice sites that inhibit migration of boron. The dopant migration resistant layer can be implanted into the screening region or provided as an in-situ doped epitaxial layer.

In certain embodiments, a threshold voltage set region **111** is positioned above the screening region **112**, and is typically formed as a thin doped layer. The threshold voltage set region **111** can be either adjacent to the screening region or vertically offset from the screening region. In certain embodiments, the threshold voltage set region **111** is formed by delta doping, controlled in-situ deposition, or atomic layer deposition. In alternative embodiments, the threshold voltage set region **111** can be formed by way of an in-situ doped epitaxial layer that is grown above the screening region **112**, or by epitaxial growth of a layer of silicon followed by diffusion of dopant atoms from the screening region. In certain embodiments, suitably varying dopant concentration, and thickness of the threshold voltage set region **111**, as well as separation of the threshold voltage set region **111** from the gate dielectric **128** and the screening region **112** allows for slight adjustments of threshold voltage in the operating transistor. In certain embodiments, the threshold voltage set region **111** can have a